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Soumya Banerjee

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EXAMINER

JOHNSON, BRIAN P

ART UNIT

PAPER NUMBER

2183

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/698,061	Applicant(s) BANERJEE ET AL.	
	Examiner BRIAN P. JOHNSON	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 February 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-46 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-46 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-46 are pending.

Papers Filed

2. Examiner acknowledges receipt remarks and amendments filed 26 February 2008.

Claim Objections

1. Claims 23-30 and 45-46 disclose a “computer readable storage medium.” There is no support in the specification for such media. Examiner recommends the following change to paragraph [0068] to clarify the issue:

Such software can be disposed in any known computer usable medium including computer readable storage medium such as semiconductor, magnetic disk, optical disc (e.g., CD-ROM, DVD-ROM, etc.) and as a computer data signal embodied in a computer usable (e.g., readable) transmission medium (e.g., carrier wave or any other medium including digital, optical, or analog-based medium). As such, the software can be transmitted over communication networks including the Internet and intranets.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 7-12, 15-20, 23-26, 29-41, 43, and 44-46 are rejected under 35 U.S.C. 102(b) as being anticipated by Trivedi (U.S. Patent No. 6,430,674).

3. As per claim 1, Trivedi discloses an instruction fetch unit for a processor (fig. 3 reference 302a, comprising: a first recorder (fig. 3 reference 306 or "circuitry" discussed on col 4 lines 17-33); and a second recorder coupled to the first recoder (fig. 3 reference 302c), wherein the first recoder passes information regarding (fig. 3 "speculative wake up" or "mode select signal" from col 4 lines 17-33) a first instruction belonging to a first instruction set architecture to the second recoder, and the second recoder recodes a second instruction belonging to the first instruction set architecture using the passed information to form a recoded instruction belonging to a second instruction set architecture (col 4 lines 17-33).

3. As per claim 2, Trivedi discloses the instruction fetch unit of claim 1, further comprising: an instruction-staging unit coupled to the first recoder and the second recoder that dispatches an instruction from an instruction cache to one of the first recoder and the second recoder (col 3 line 62 to col 4 lines 10)

4. As per claim 3, Trivedi discloses the instruction fetch unit of claim 1, wherein the processor executes instructions having X-bits and belonging to a first instruction set and instructions having Y-bits and belonging to a second instruction set, Y being greater than X, and wherein the first recoder and the second recoder recode an instruction belonging to one of the first instruction set and the second instruction set to form a recoded instruction having at least Y-bits. (col 3 lines 33-46)

5. As per claim 4, Trivedi discloses the instruction fetch unit of claim 3, wherein each instruction of the first instruction set has 16-bits and each instruction of the second instruction set has 32-bits. (col 3 lines 33-46)

6. As per claim 7, Trivedi discloses the instruction fetch unit of claim 3, wherein the first instruction set includes a mode-switching instruction that switches the operating mode of the processor, and wherein the first recoder passes one or more bits to the second recoder thereby allowing the second recoder to recode the mode-switching instruction. (Col. 4 lines 17-33)

7. As per claim 8, Trivedi discloses the instruction fetch unit of claim 7, wherein the one or more bits are concatenated to at least one bit of the mode-switching instruction. (Col. 4 lines 17-33)

8. As per claim 9, Trivedi has taught a processor employing the fetch unit of claim 1, consequently claim 9 is rejected for the same reasons set forth in the rejection of claim 1 above.

9. As per claim 10, Trivedi has taught a processor employing the fetch unit of claim 2, consequently claim 10 is rejected for the same reasons set forth in the rejection of claim 2 above.

10. As per claim 11, Trivedi has taught a processor employing the fetch unit of claim 3, consequently claim 11 is rejected for the same reasons set forth in the rejection of claim 3 above.

11. As per claim 12, Trivedi has taught a processor employing the fetch unit of claim 4, consequently claim 12 is rejected for the same reasons set forth in the rejection of claim 4 above.

12. As per claim 15, Trivedi has taught a processor employing the fetch unit of claim 7, consequently claim 15 is rejected for the same reasons set forth in the rejection of claim 7 above.

13. As per claim 16, Trivedi has taught a processor employing the fetch unit of claim 8, consequently claim 16 is rejected for the same reasons set forth in the rejection of claim 8 above.

14. As per claim 17, Trivedi has taught a processing system employing the fetch unit of claim 1, consequently claim 17 is rejected for the same reasons set forth in the rejection of claim 1 above.

Art Unit: 2183

15. As per claim 18, Trivedi has taught a processing system employing the fetch unit of claim 2, consequently claim 18 is rejected for the same reasons set forth in the rejection of claim 2 above.

16. As per claim 19, Trivedi has taught a processing system employing the fetch unit of claim 3, consequently claim 19 is rejected for the same reasons set forth in the rejection of claim 3 above.

17. As per claim 20, Trivedi has taught a processing system employing the fetch unit of claim 4, consequently claim 20 is rejected for the same reasons set forth in the rejection of claim 4 above.

18. As per claim 23, Trivedi has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 1, consequently claim 23 is rejected for the same reasons set forth in the rejection of claim 1 above.

19. As per claim 24, Trivedi has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 2, consequently claim 24 is rejected for the same reasons set forth in the rejection of claim 2 above.

Art Unit: 2183

20. As per claim 25, Trivedi has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 3, consequently claim 25 is rejected for the same reasons set forth in the rejection of claim 3 above.

21. As per claim 26, Trivedi has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 4, consequently claim 26 is rejected for the same reasons set forth in the rejection of claim 4 above.

22. As per claim 29, Trivedi has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 7, consequently claim 29 is rejected for the same reasons set forth in the rejection of claim 7 above.

23. As per claim 30, Trivedi has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 8, consequently claim 30 is rejected for the same reasons set forth in the rejection of claim 8 above.

24. As per claim 31, Trivedi discloses a method for recoding instructions for execution by a computer readable medium comprising a microprocessor core, comprising:

(a) fetching an expand instruction (prefix instruction) and an expandable instruction (target instruction) from an instruction cache (col 3 line 62 to col 4 lines 10);

(b) dispatching the expand instruction to a first recoder and dispatching the expandable instruction to a second recoder; (col 4 lines 17-33)

(c) generating at the first recoder at least one information bit based on the expand instruction; (col 4 lines 17-33);

and (d) recoding the expandable instruction using the at least one information bit generated to form a recoded instruction belonging to a second instruction set architecture. (Col. 4 lines 17-33)

25. As per claim 32, Trivedi discloses the method of claim 31, wherein step (a) comprises:

(i) fetching the expand instruction during a first clock cycle of the computer readable medium comprising a microprocessor core; and

(ii) fetching the expandable instruction during a subsequent clock cycle of the computer readable medium comprising a microprocessor core (fig. 3 and col 4 lines 17-33)

26. As per claim 33, Trivedi discloses the method of claim 31, wherein the at least one information bit based on the expand instruction is generated at the first recoder during a first clock cycle of the processor, and the expandable instruction is recoded at the second recoder during a second clock cycle of the computer readable medium comprising a microprocessor core (col 4 lines 17-33 and fig. 3)

Art Unit: 2183

27. As per claim 34, Trivedi discloses the method of claim 33, further comprising a step between steps (c) and (d) of:

storing the at least one information bit generated at the first recoder in an information storage buffer. (col 4l inse 17-33)

28. As per claim 35, Trivedi discloses a method for recoding instructions for execution by a processor, comprising:

fetching a plurality of instructions from an instruction cache (col 3 line 62 to col 4 lines 10), wherein the plurality of instructions includes a first instruction belonging to a first instruction set architecture and a second instruction belonging to the first instruction set architecture, and the first instruction is different from the second instruction (col 4 lines 17-33)

dispatching the first instruction to a first recoder and the second instruction to a second recoder; (fig. 3)

and recoding the first and second instructions within a single clock cycle so as to form recoded instructions belonging to a second instruction set architecture for each of the first instruction and the second instruction (col 4 lines 17-33).

29. As per claim 36, Trivedi discloses the method of claim 35, wherein the recoding of the second instruction is performed using information from the first instruction. (Col. 4 lines 17-33)

Art Unit: 2183

30. As per claim 37, Trivedi discloses the method of claim 35, further comprising forwarding information from the first recoder to the second recoder, such information used by the second recoder to perform a recoding operation. (Col. 4 line s17-33)

31. As per claim 38, Trivedi discloses an instruction fetch unit for a processor comprising:

a first recoder (Fig. 3 wake up signal and col 4 lines 17-33);

and a second recoder (fig 3 reference 302c) which operates in parallel with the first recoder;

wherein the first recoder recodes instructions belonging to a first instruction set architecture within a single clock cycle so as to form recoded instructions belonging to a second instruction set architecture (col 4 lines 17-33)

32. As per claim 39, Trivedi discloses the instruction fetch unit of claim 38, wherein the second recoder recodes the second instruction using information from the first instruction. (Col. 12 lines 21-31)

33. As per claim 40, Trivedi discloses the instruction fetch unit of claim 39, wherein the first recoder is coupled to the second recoder. (fig. 3)

34. As per claim 41, Trivedi discloses the instruction fetch unit of claim 1, wherein the first instruction is used to enlarge a field of the second instruction and the information is at least one bit of the first instruction. (col 3 lines 33-46)

35. As per claim 43, Trivedi has taught a processor employing the fetch unit of claim 41, consequently claim 43 is rejected for the same reasons set forth in the rejection of claim 41 above.

36. As per claim 45, Trivedi has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 41, consequently claim 45 is rejected for the same reasons set forth in the rejection of claim 41 above.

4. As per claim 46, Trivedi has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 42, consequently claim 46 is rejected for the same reasons set forth in the rejection of claim 42 above.

Claim Rejections - 35 USC § 103

5. Claims 5, 6, 13, 14, 21, 22, 27, 28, 42, and 44 rejected under 35 U.S.C. 103(a) as being unpatentable over Trivedi over Common Art.

37. As per claim 5, Trivedi discloses the instruction fetch unit of claim 3, wherein the first instruction set includes an expand instruction used to enlarge a field of an

Art Unit: 2183

expandable instruction of the first instruction set, (col 4 lines 17-33) and wherein the first recoder passes at least one bit of the expand instruction to the second recoder thereby allowing the second recoder to recode the expandable instruction. (col 4 lines 17-33 and col 3 lines 33-46)

Trivedi fails to disclose that the expandable portion is the immediate field.

Examiner takes Official Notice that expanding an instruction architecture (for example, from 32 to 64 bits) often includes expanding the immediate field.

Trivedi would have been motivate to utilize this technique to expand the architecture in such a way that the immediate field contains larger numbers, which increases the flexibly of coding.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Trivedi and incorporate the immediate field expansion of common art.

38. As per claim 6, Trivedi discloses the instruction fetch unit of claim 5, wherein the at least one bit of the expand instruction is concatenated to at least one bit of the expandable instruction. (col 4 lines 17-33 and col 3 lines 33-46)

39. As per claim 13, Trivedi has taught a processor employing the fetch unit of claim 5, consequently claim 13 is rejected for the same reasons set forth in the rejection of claim 5 above.

Art Unit: 2183

40. As per claim 14, Trivedi has taught a processor employing the fetch unit of claim 6, consequently claim 14 is rejected for the same reasons set forth in the rejection of claim 6 above.

41. As per claim 21, Trivedi has taught a processing system employing the fetch unit of claim 5, consequently claim 21 is rejected for the same reasons set forth in the rejection of claim 5 above.

42. As per claim 22, Trivedi has taught a processing system employing the fetch unit of claim 6, consequently claim 22 is rejected for the same reasons set forth in the rejection of claim 6 above.

43. As per claim 27, Trivedi has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 5, consequently claim 27 is rejected for the same reasons set forth in the rejection of claim 5 above.

44. As per claim 28, Trivedi has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 6, consequently claim 28 is rejected for the same reasons set forth in the rejection of claim 6 above.

45. As per claim 42, Trivedi discloses the instruction fetch unit of claim 41, wherein the first instruction is an expand instruction, the second instruction is an expandable instruction and the field is an immediate field. (col 3 lines 33-46)

46. As per claim 44, Trivedi has taught a processor employing the fetch unit of claim 42, consequently claim 44 is rejected for the same reasons set forth in the rejection of claim 42 above.

Response to Arguments

Applicant's arguments filed 26 February 2008 have been fully considered but they are not persuasive. Other arguments are moot due to a new grounds rejection.

Applicant argues that the term "computer readable storage medium" has sufficient antecedent basis in light of paragraph [0068]. Examiner disagrees. It is not clear whether paragraph [0068] refers to the "computer readable storage medium" found in the claims. The amendment suggested above will clarify the issue.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2183

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/

Supervisory Patent Examiner, Art Unit 2183